

	Search Text
1	(hard adj marco hardmacro) same CPU same memory adj controller
2	(hard adj marco hardmacro) same CPU same memory adj controller
3	(hard adj marco hardmacro macro\$7) same CPU same memory adj controller
4	(hard adj marco hardmacro macro\$7) same CPU same memory adj controller and register same (hard adj marco hardmacro macro\$7)
5	(hard adj marco hardmacro macro\$7) same CPU same memory adj controller and register same (hard adj marco hardmacro macro\$7) and (second another) near4 memory near4 controller
6	(hard adj marco hardmacro macro\$7) same (CPU processor microprocessor micro adj processor) same memory adj controller
7	(hard adj marco hardmacro macro\$6) same (CPU processor microprocessor micro adj processor) same memory adj controller and register same (hard adj marco hardmacro macro\$6) and (second another plural\$4 multi\$6 ) near4 memory near4 controller
8	(core) same (CPU processor microprocessor micro adj processor) same memory adj controller
9	(core) same (CPU processor microprocessor micro adj processor) same memory adj controller and register same (hard adj marco hardmacro macro\$6) and (second another plural\$4 multi\$6 ) near4 memory near4 controller
10	(core macro hardmacro cpu processor microprocessor micro adj processor) and (second adj memory adj controller )
11	(core macro hardmacro cpu processor microprocessor micro adj processor) and (second adj memory adj controller ) and (interfa\$4) and (i/o input/output input near3 output)
12	(core macro hardmacro cpu processor microprocessor micro adj processor) and (second adj memory adj controller ) and (interfa\$4) and (i/o input/output input near3 output) and (pad buffer driver) same (memory or controller)

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1	second adj memory adj controller
2	second adj memory adj controller and @ad<"20031112"
3	second adj memory adj controller and @ad<"20031112" and (hard\$7 macro)
4	second adj memory adj controller and @ad<"20031112" and (hardmacro hard adj macro hardcore)
5	second adj memory adj controller and @ad<"20031112" and (hardmacro hard adj macro hardcore core)
6	second adj memory adj controller and @ad<"20031112" and (hardmacro hard adj macro hardcore core) and interface
7	(memory adj controller ) with (plural\$6) and @ad<"20031112" and (hardmacro hard adj macro hardcore core) and interface
8	(memory adj controller ) with (plural\$6) and @ad<"20031112" and (hardmacro hard adj macro hardcore core) and interface same (memory adj controller )
9	(memory adj controller ) with (plural\$6) and @ad<"20031112" and (hardmacro hard adj macro hardcore core) and interface same (memory adj controller ) and register
10	(memory adj controller ) with (plural\$6) and @ad<"20031112" and (hardmacro hard adj macro hardcore core) and interface same (memory adj controller ) and register and (cpu processor microprocessor)
11	(memory adj controller ) with (plural\$6) and @ad<"20031112" and (hardmacro hard adj macro hardcore core) and interface same (memory adj controller ) and register and (cpu processor microprocessor) and (wir\$4 path trace route connect\$4 interconnect\$4) same (length distance) same (memory adj controller )
12	(memory adj controller ) same (cpu processor microprocessor) and @ad<"20031112" and interface same (memory adj controller ) and register and (cpu processor microprocessor) and (wir\$4 path trace route connect\$4 interconnect\$4) same (length distance) same (memory adj controller ) and interface same (memory )
13	(memory adj controller ) same (cpu processor microprocessor) and @ad<"20031112" and interface same (memory adj controller ) and register and (cpu processor microprocessor) and (wir\$4 path trace route connect\$4 interconnect\$4) same (length distance) same (memory adj controller ) and interface same (memory ) and address\$4 same memory
14	(memory adj controller ) same (cpu processor microprocessor) and @ad<"20031112" and interface same (memory adj controller ) and register and (cpu processor microprocessor) and ((wir\$4 path trace route connect\$4 interconnect\$4) with (length distance)) same (memory adj controller ) and interface same (memory ) and address\$4 same memory
15	(memory adj controller ) and (cpu processor microprocessor) and @ad<"20031112" and interface same (memory adj controller ) and register and ((wir\$4 path trace route connect\$4 interconnect\$4) with (length distance)) same (memory adj controller ) and interface same (memory ) and address\$4 same memory and ddr
16	second adj memory adj controller and @ad<"20031112" and ddr
17	second adj memory adj controller and @ad<"20031112" and sram
18	second adj memory adj controller and @ad<"20031112" and sram and register
19	second adj memory adj controller and @ad<"20031112" and interfa\$4 and (ddr sram)

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20	second adj memory adj controller and @ad<"20031112" and interfa\$4 and (ddr sdram) and register and (cpu processor microprocessor) and length and delay\$4
21	second adj memory adj controller and @ad<"20031112" and interfa\$4 and (ddr sdram) and register and (cpu processor microprocessor) and ((wir\$4 path trace route connect\$5 track interconnect\$4) with (length delay distance))
22	(memory adj controller ) with (plural\$6 multi\$5 second) and (hardmacro macro core) and interfac\$5 same (memory adj controller ) and register and (cpu processor microprocessor)
23	(memory adj controller ) with (plural\$6 multi\$5 second) and (hardmacro macro core) and interfac\$5 same (memory adj controller ) and register and (cpu processor microprocessor) and (i/o input/output input near3 output)
24	(memory adj controller ) with (plural\$6 multi\$5 second) and (hardmacro macro core) and interfac\$5 same (memory adj controller ) and register and (cpu processor microprocessor) and (i/o input/output input near3 output) same (pad buffer driver)
25	(memory adj controller ) with (plural\$6 multi\$5 second) and (hardmacro macro core) and interfac\$5 same (memory adj controller ) and register and (cpu processor microprocessor) and (i/o input/output input near3 output) same (interfac\$6)
26	(memory adj controller ) with (plural\$6 multi\$5 second) and (hardmacro macro core) and interfac\$5 same (memory adj controller ) and register and (cpu processor microprocessor) and (i/o input/output input near3 output) same (interfac\$6) and @ad<"20031112"